

REMARKS/ARGUMENTS

In the Office Action mailed September 21, 2007, claims 1-5, 7, and 8 were rejected. Additionally, the drawings and specification were objected to. In response, Applicants hereby request reconsideration of the application in view of the amended claims and the below-provided remarks.

For reference, claims 1-8 are amended, and claims 9-11 are added. No claims are canceled. In particular, claims 1 and 8 are amended to clarify the limitation related to unrestricted mapping. These amendments are supported in the specification, for example, by the subject matter described at page 5, line 29, through page 6, line 2, and in the drawings, for example, by the illustration of Fig. 2. Claim 4 is amended to clarify the limitation related to reduction mapping. This amendment is supported in the specification, for example, by the subject matter described at page 7, lines 1-2. The preambles of claims 1-8 are also amended to recited definite and indefinite articles for the integrated circuit and the method.

New claim 9 is directed to distributing faulty memory modules evenly over a plurality of banks. This amendment is supported in the specification, for example, by the subject matter described at page 5, line 29, through page 6, line 2. New claim 10 is directed to unrestricted remapping at a block/line granularity. This amendment is supported in the specification, for example, by the subject matter described at page 8, lines 1-5. New claim 11 is directed to remapping over multiple indices. This amendment is supported in the specification, for example, by the subject matter described at page 8, lines 19-27.

Objections to the Drawings

The drawings are objected to because there are no reference characters. Although the Office Action references 37 C.F.R. 1.87(p) as the basis for this rejection, Applicants respectfully note that the indicated rule does not exist. Rather, it appears that 37 C.F.R. 1.84(p) is the rule that the Office Action intended to reference. However, rule 1.84(p) merely sets standards for reference characters that are used, but rule 1.84(p) does not require that numeral reference characters be used (even though they are preferred).

Hence, it appears that the present objection to the drawings does not have a proper basis in the rules, despite the Office Action's assertion.

Moreover, rule 1.83(a) recognizes that the content of the drawings may be presented in the form of graphical drawing symbols and labeled representations (e.g., a labeled rectangular box). Therefore, since the drawings of the present application present labeled rectangular boxes, which are acceptable under the rules, Applicants respectfully request that the objection to the drawings be withdrawn.

Objections to the Specification

The specification is objected to for various informalities. Applicants appreciate the Examiner's attention to the language of the specification. Applicants submit that various portions of the specification are amended to address the indicated informalities, as well as to clarify additional portions of the specification. Accordingly, Applicants respectfully request that the objections to the specification be withdrawn.

No *Prima Facie* Rejection

As a preliminary matter, Applicants note that the Office Action does not present a substantive rejection of claim 6. Although the Office Action Summary indicates that claims 1-8 are rejected, the body of the Office Action does not specifically reference claim 6. It appears that the Examiner may have inadvertently presented two rejections for claim 5, with the intention of addressing the limitations of claim 6 in one of the rejections. Nevertheless, Applicants respectfully request clarification of the rejections by the Examiner. Furthermore, Applicants respectfully submit that the next action should not be made final if it includes a rejection specific to claim 6.

Claim Rejections under 35 U.S.C. 112

Claim 4 was rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. In particular, the Office Action states that "reduction mapping" is not well known in the art and is not explained clearly enough in the specification.

As a preliminary matter, Applicants note that the Office Action asserts entirely inconsistent assertions with respect to the reduction mapping limitation of claim 4. Within the context of the rejection of claim 4 under 35 U.S.C. 112, first paragraph, the Office Action states that reduction mapping “is not well known in the art” (emphasis added). In contrast, within the context of the rejection of claim 4 under 35 U.S.C. 103(a), the Office Action states that reduction mapping “was notoriously well known in the art” (emphasis added). Hence, the Office Action asserts two contradictory assertions—that reduction mapping is not well known and that reduction mapping is notoriously well known. While it appears that these contradictory assertions may have been presented inadvertently, Applicants request that the Examiner clarify a single, consistent position that the Examiner wishes to assert in regard to a rejection, if any, directed to the reduction mapping limitation of claim 4.

In the event that the asserted position is based on the purported common knowledge of reduction mapping, then the rejection of claim 4 under 35 U.S.C. 112, first paragraph, should be withdrawn because the common knowledge of reduction mapping should be sufficient to demonstrate enablement of the reduction mapping limitation. Alternatively, if the asserted position is based on the lack of common knowledge of reduction mapping, then the rejection of claim 4 under 35 U.S.C. 103(a) should be withdrawn because the assertion of common knowledge is the basis of the rejection.

Despite the apparent question as to the common knowledge, or lack thereof, of reduction mapping, Applicants submit that the reduction mapping limitation is supported by the subject matter described in the specification. In particular, the specification refers to reduction mapping which uses less output signals than input signals. See, page 7, lines 1-2, and the surrounding description. Additionally, Applicants submit that claim 4 is amended to clarify the reduction mapping limitation. Accordingly, Applicants submit the term “reduction mapping” in claim 4 complies with the enablement requirement and respectfully requests that the rejection of claim 4 under 35 U.S.C. 112, first paragraph, be withdrawn.

Claim Rejections under 35 U.S.C. 102/103

Claims 1, 2, 4, 5, 7, and 8 were rejected under 35 U.S.C. 102(b) as being anticipated by Lefsky (U.S. Pat. No. 5,019,971, hereinafter Lefsky). In the alternative, claim 4 was rejected under 35 U.S.C. 103(a) as obvious over common knowledge in the art. Claim 5 was also rejected under 35 U.S.C. 103(a) as being unpatentable over Asher (U.S. Pat. No. 6,671,822, hereinafter Asher) in view of Kramer (U.S. Pat. No. 4,868,869, hereinafter Kramer). Additionally, claims 1-3 and 8 were rejected under 35 U.S.C. 102(e) as being unpatentable over Asher. However, Applicants respectfully submit that these claims are patentable over Lefsky, Asher, Kramer, and the common knowledge in the art for the reasons provided below.

Independent Claim 1

Claim 1 recites “remapping means (RM, MapRAM) for performing an unrestricted remapping within said plurality of memory modules, wherein the unrestricted remapping permits remapping the memory modules from a first bank of memory modules to a second bank of memory modules” (emphasis added).

In contrast, Lefsky does not disclose remapping memory modules from one bank to another bank of memory modules. Lefsky merely describes tracking which cache cells are faulty. Lefsky, Abstract. In particular, Lefsky describes a force bit control module to use force bits associated with each cache cell. Lefsky, col. 7, lines 63-64. The force bit indicates whether or not a cache cell is operational. Lefsky, col. 5, lines 11-12. If the cache cell is operational, then it may be used for read/write operations; otherwise, if the cache cell is faulty (as indicated by the set force bit), then the defective cache cell is ignored and not used to store data. Lefsky, col. 5, lines 13-18. In other words, the force bit merely indicates that whether or not the corresponding cache cell is faulty (the force bit is set) or operational (the force bit is reset).

Lefsky describes “mapping” cache cells for which the corresponding force bit is set. Lefsky, col. 3, lines 16-19. However, this mapping of the force bits is not the same as the remapping functionality recited in claim 1 because the mapping of Lefsky is merely related to tracking which force bits are set or reset, in order to determine whether or not the corresponding cache cells are operational. However, Lefsky does not describe

any type remapping in which a memory module of a first bank might be remapped to a second bank. As a further example of remapping, the present application describes the embodiment of Fig. 2 and explains that ways, or memory modules, from banks 2, 4, and 7 may be remapped to bank 0. While this example is not mentioned in the claims, it might help to illustrate the function of remapping, or making memory modules available from one bank to another bank within the cache. This type of remapping contrasts with the mapping of Lefsky because Lefsky merely maps, or keeps track of, the force bits associated with faulty cache cells, but does not remap other cache cells, or make them available within a bank, to compensate for the faulty cache cells. Therefore, Lefsky does not disclose all of the limitations of the claim because Lefsky does not disclose remapping memory modules between banks of memory modules, as recited in the claim. Accordingly, Applicants respectfully submit claim 1 is patentable over Lefsky because Lefsky does not disclose all of the limitations of the claim.

Asher also fails to disclose all of the limitations of the claims. In particular, Asher does not describe remapping memory modules from a first bank of memory modules to a second bank of memory modules. Asher merely describes reserving one or more ways distributed across multiple banks within a cache so that the reserved way may be substituted for a defective way in the corresponding bank. In other words, Asher merely describes remapping ways within the same bank. Therefore, Asher does not disclose all of the limitations of the claim because Asher does not disclose remapping memory modules between banks of memory modules, as recited in the claim. Accordingly, Applicants respectfully submit claim 1 is patentable over Asher because Asher does not disclose all of the limitations of the claim.

Independent Claim 8

Applicants respectfully assert independent claim 8 is patentable over Lefsky and Asher at least for similar reasons to those stated above in regard to the rejections of independent claim 1. In particular, claim 8 recites “performing an unrestricted remapping within said plurality of memory modules, wherein the unrestricted remapping permits remapping the memory modules from a first bank of memory modules to a second bank of memory modules” (emphasis added).

Here, although the language of claim 8 differs from the language of claim 1, and the scope of claim 8 should be interpreted independently of claim 1, Applicants respectfully assert that the remarks provided above in regard to the rejections of claim 1 also apply to the rejections of claim 8. Accordingly, Applicants respectfully assert claim 8 is patentable over Lefsky and Asher because Lefsky and Asher do not disclose remapping memory modules between banks of memory modules, as recited in the claim.

Dependent Claims

Claims 2-7 and 9-11 depend from and incorporate all of the limitations of independent claim 1. Applicants respectfully assert claims 2-7 and 9-11 are allowable based on an allowable base claim. Additionally, each of claims 2-7 and 9-11 may be allowable for further reasons.

CONCLUSION

Applicants respectfully request reconsideration of the claims in view of the amendments and remarks made herein. A notice of allowance is earnestly solicited.

At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account **50-3444** pursuant to 37 C.F.R. 1.25. Additionally, please charge any fees to Deposit Account **50-3444** under 37 C.F.R. 1.16, 1.17, 1.19, 1.20 and 1.21.

Respectfully submitted,

/Jeffrey T. Holman/

Date: December 21, 2007

Jeffrey T. Holman
Reg. No. 51,812

Wilson & Ham
PMB: 348
2530 Berryessa Road
San Jose, CA 95132
Phone: (925) 249-1300
Fax: (925) 249-0111